In the Claims:

Claims 1-20 (canceled)

Please cancel claims 21-37

Please add the claims 38 - 52 as follows:

38. A processor comprises:
a general purpose processor that coordinates system functions; and
a plurality of microengines that support multiple hardware threads.

39. The processor of claim 1 wherein the general purpose processor load microcontrol programs in the plurality of microcontrol engines.

40. The processor of claim 1 further comprising a memory control system.

41. The processor of claim 1 wherein the memory control system comprises a synchronous dynamic random access memory controller that optimizes memory references based on whether the memory references are directed to an even bank or an odd bank of memory.

42. The processor of claim 1 wherein the memory control system comprises a static random access memory controller that optimizes memory references based upon whether the memory references are read references or write references.

43. The processor of claim 1 wherein each of the plurality of microengines employ hardware-based context swapping amongst a plurality of threads that are independently executable within each of the microengines.

44. The processor of claim 1 further comprising a high speed bus interface that couples the processor to a communication bus.

45. The processor of claim 1 further comprising a bus interface that couples the processor to a computer system bus.

46. The processor of claim 1 further comprising an internal bus arrangement to couple shared resources in the processor to the plurality of microengines.

47. The processor of claim 9 wherein the internal bus arrangement to couple shared resources, comprises:

a first bus to couple the general purpose processor to the plurality of microengines.

48. The processor of claim 9 wherein the internal bus arrangement to couple shared resources, comprises:

a translator device that tranlates requests from the general purpose processor to the microengines; and

a first bus to couple the general purpose processor to the plurality of microengines.

49. The processor of claim 3 wherein the internal bus arrangement to couple shared resources, comprises:

a translator device that tranlates requests from the general purpose processor to the microengines; and

a first bus to couple the general purpose processor to the plurality of microengines; and

a second bus to couple the general purpose processor to the memory control system.

50. The processor of claim 11, further comprising a third bus to couple the microengines to external bus interfaces.

51. The processor of claim 8 wherein the shared resources comprise:

a memory controller for controlling access to low latency memory;

a memory controller for controlling an access to high bandwidth memory;

a bus interface for controlling access to a communications bus; and

a bus interface for controlling access to a computer bus.

52. The processor of claim 1 wherein each one of the microengines includes a program counter to uniquely identify a position of a thread during execution in the microengine.